


# B450M S2H V2

**Revision :1.0**

PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU DDR4 MEMORY
05	CPU DDI, CONTROL
06	CPU GFX, GPP, SB, GND
07	CPU MISC
08	CPU POWER
09	CPU CLK, USB3, SPI ,LPC
10	DDR4 CHANNEL A
11	DDR4 CHANNEL B
12	PM CLK, SPI, MISC
13	PM USB
14	PM SATA, GPP
15	PM POWER, GND
16	PCIEx16 ,PCIEx1 Slot
17	IT8686
18	F_USB ,F_USB30, R_USB30, KB_MS_USB
19	A_VDD1V8, A_VDDPS5
20	ALC887 CODEC
21	AUDIO JACK
22	POWER SEQ, A_VDDP
23	ATX , F_PANEL
24	PWM ISL95712
25	VCORE MOS

[illegible]

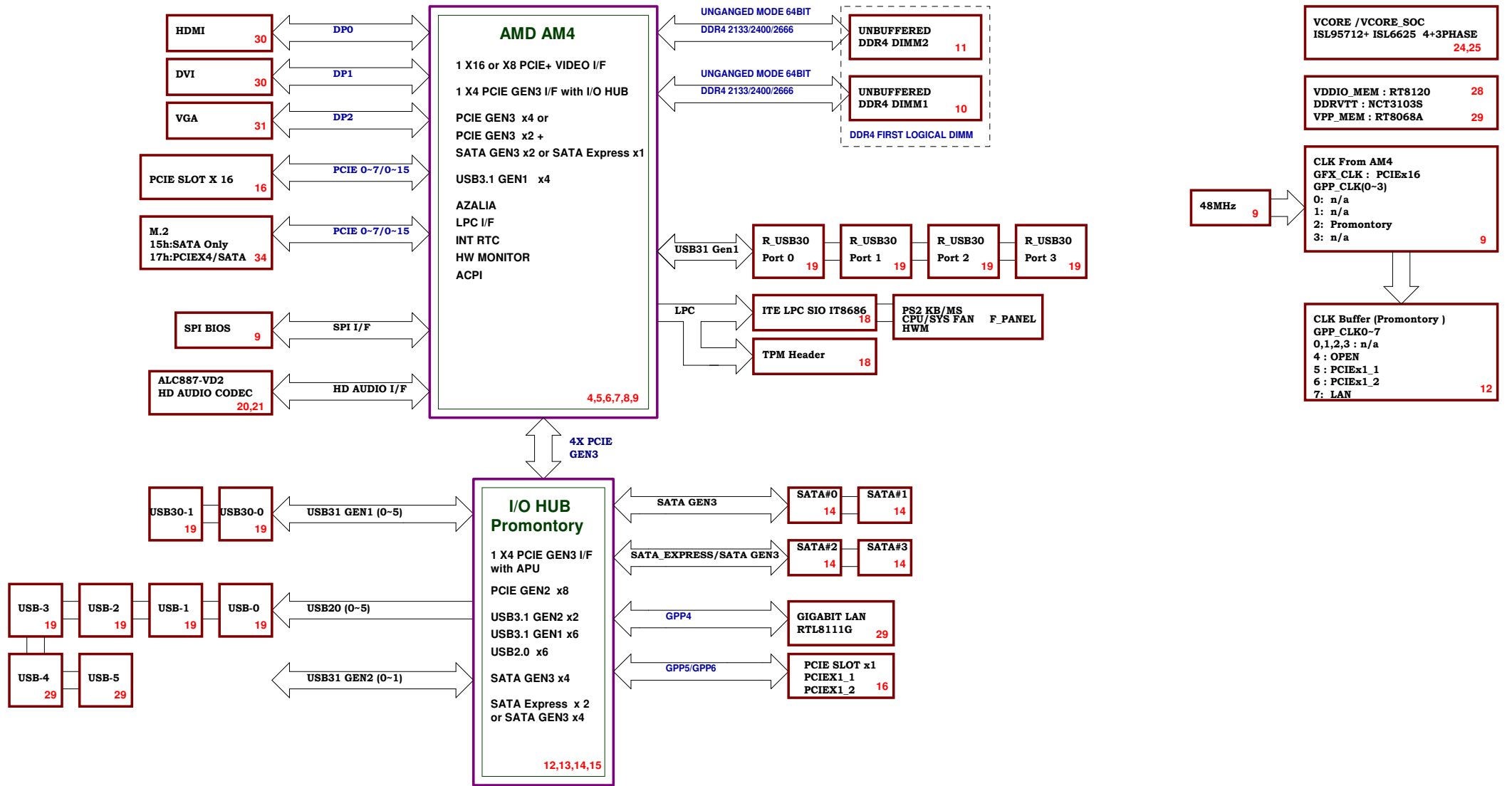
**2015.12.30--B.L**

			
<b>COVER SHEET</b>			
Size	Custom	Document Number <b>B450M S2H V2</b>	Rev <b>1.0</b>
Date: <b>Tuesday, August 25, 2020</b>		Sheet <b>1</b> of <b>35</b>	



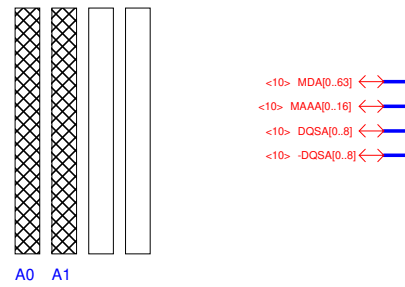
[illegible][illegible][illegible][illegible][illegible][illegible][illegible]



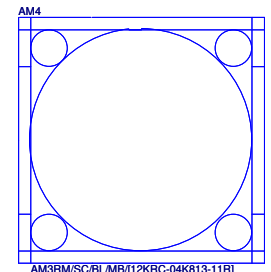




MEM CHA



<10> MDA[0..63] <=> MDA[0..63]  
<10> MAAA[0..16] <=> MAAA[0..16]  
<10> DQSA[0..8] <=> DQSA[0..8]  
<10> -DQSA[0..8] <=> -DQSA[0..8]



AM3RM/SC/BLMB[12KRC-04K813-11R]

<11> MDB[0..63] <=> MDB[0..63]  
<11> MAAB[0..16] <=> MAAB[0..16]  
<11> DQSB[0..8] <=> DQSB[0..8]  
<11> -DQSB[0..8] <=> -DQSB[0..8]

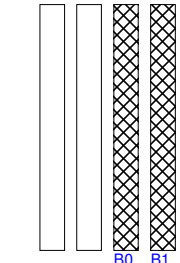
**GIGABYTE**™

Title: **APU DDR4**

Size: **Custom** Document Number: **B450M S2H V2** Rev: **1.0**

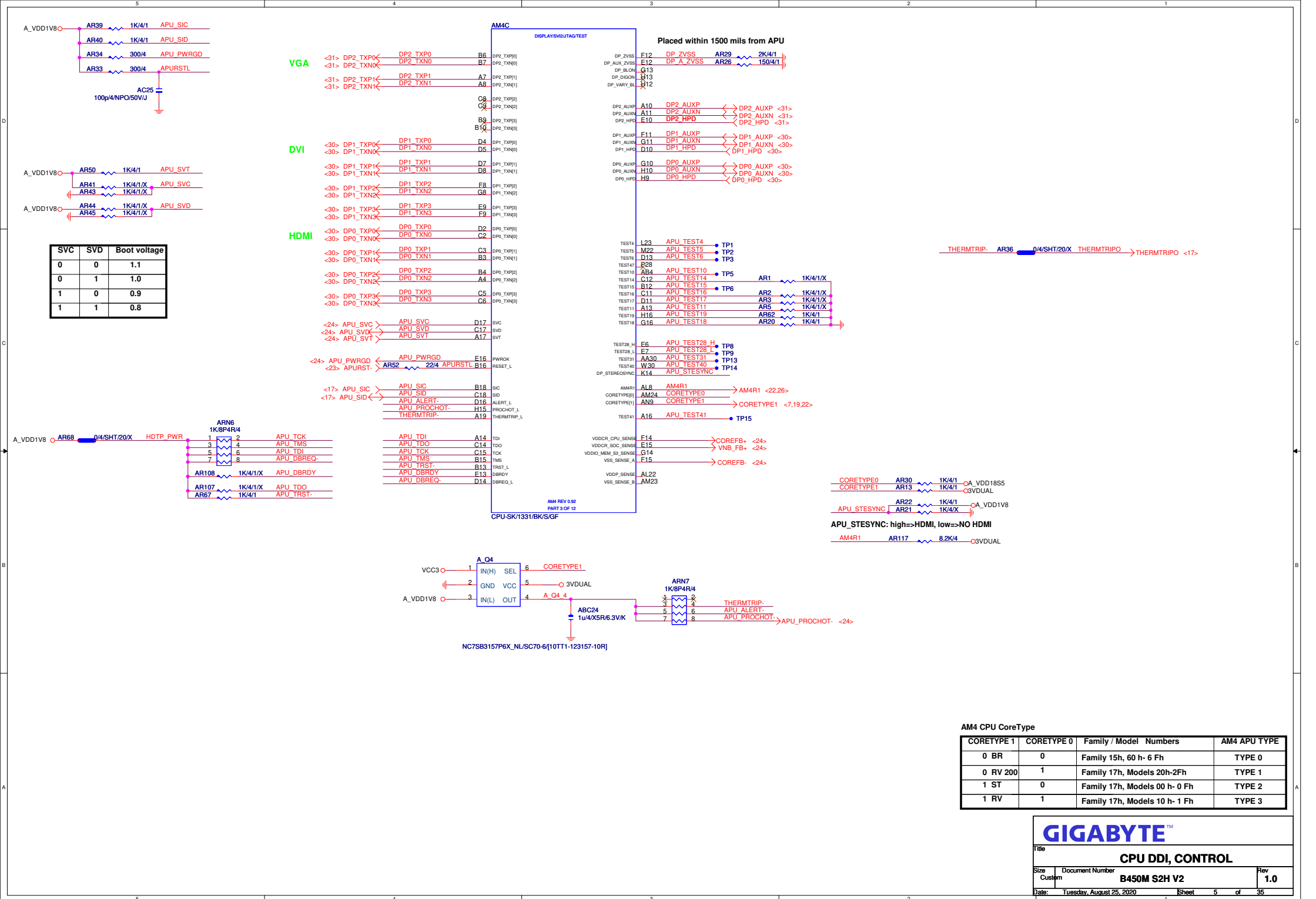
Date: **Tuesday, August 25, 2020** Sheet: **4** of **35**

MEM CHB

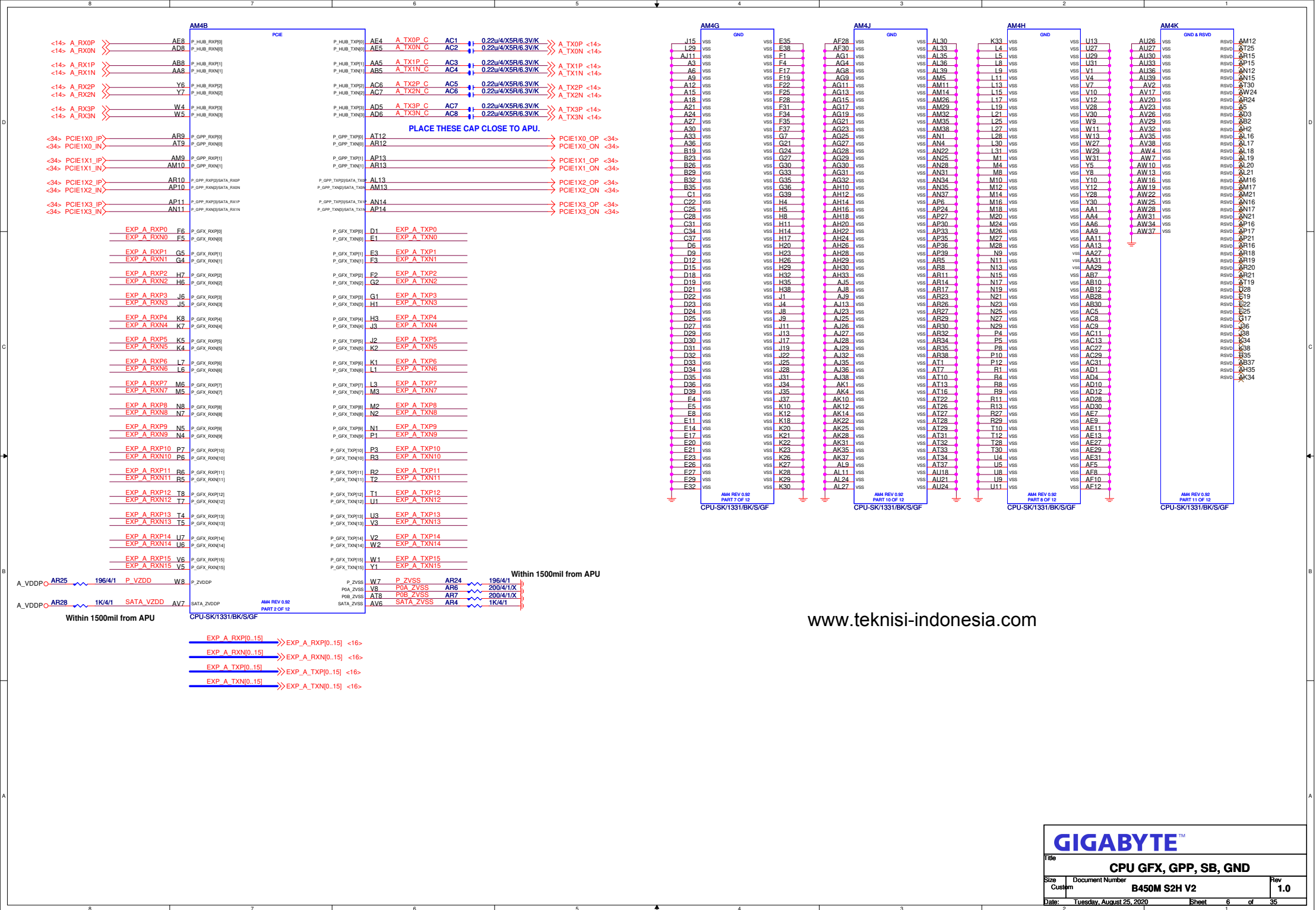


MB\_ZVDDIO\_MEM\_SS Y36 MB\_ZVSS AR49 39.2/41 OVDDIO\_MEM  
Place within 1" of APU.





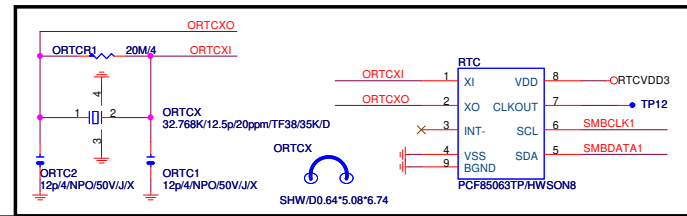






[illegible]

TEST0	TEST1	TEST2	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.



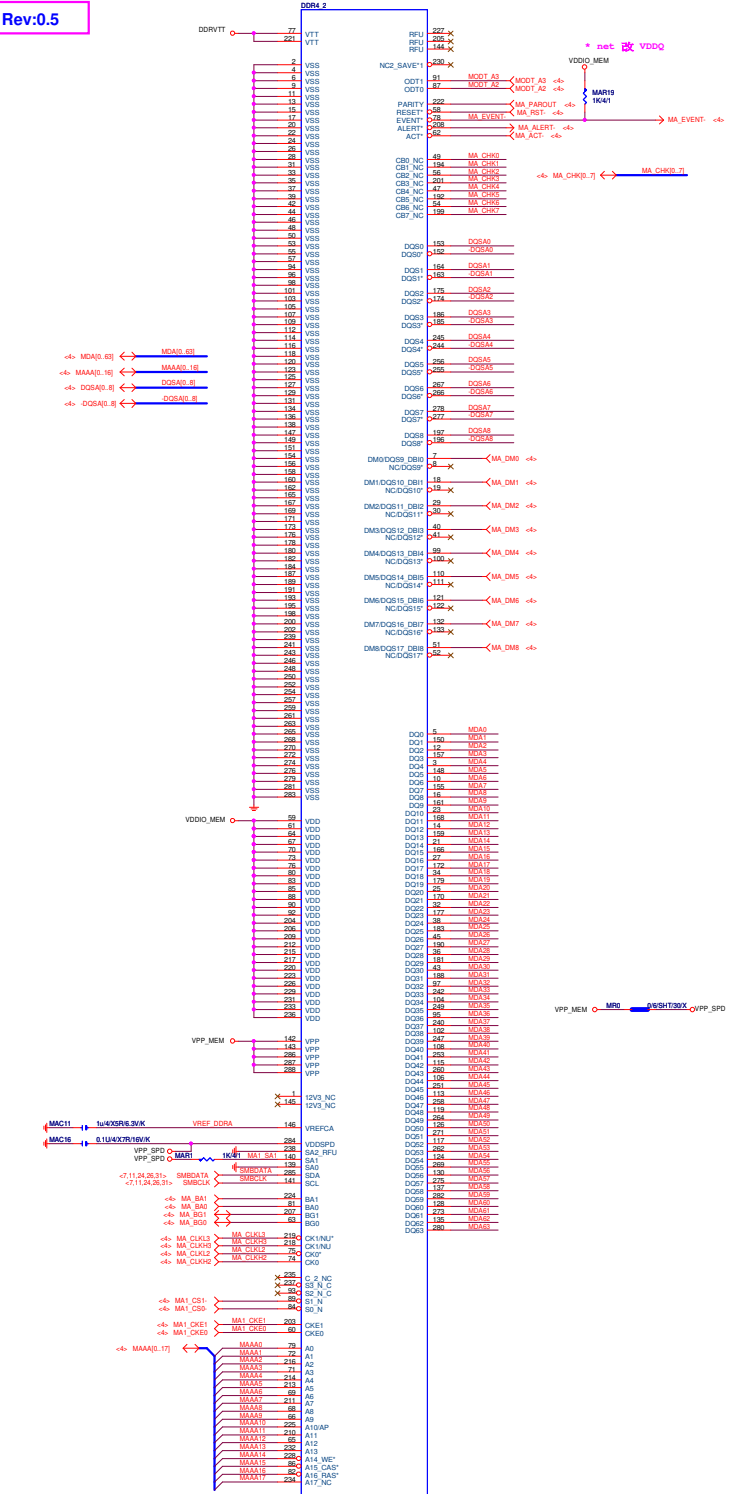












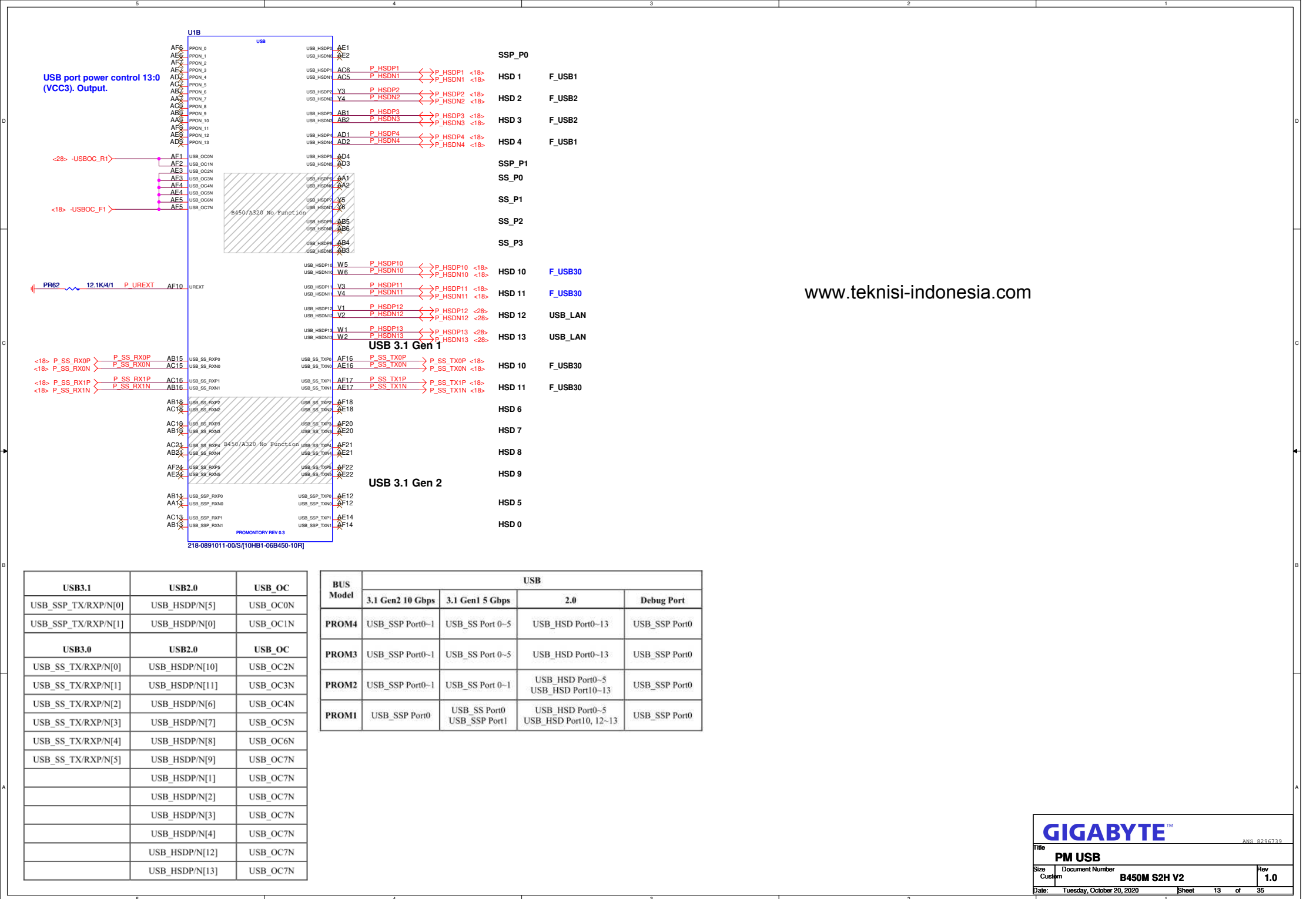




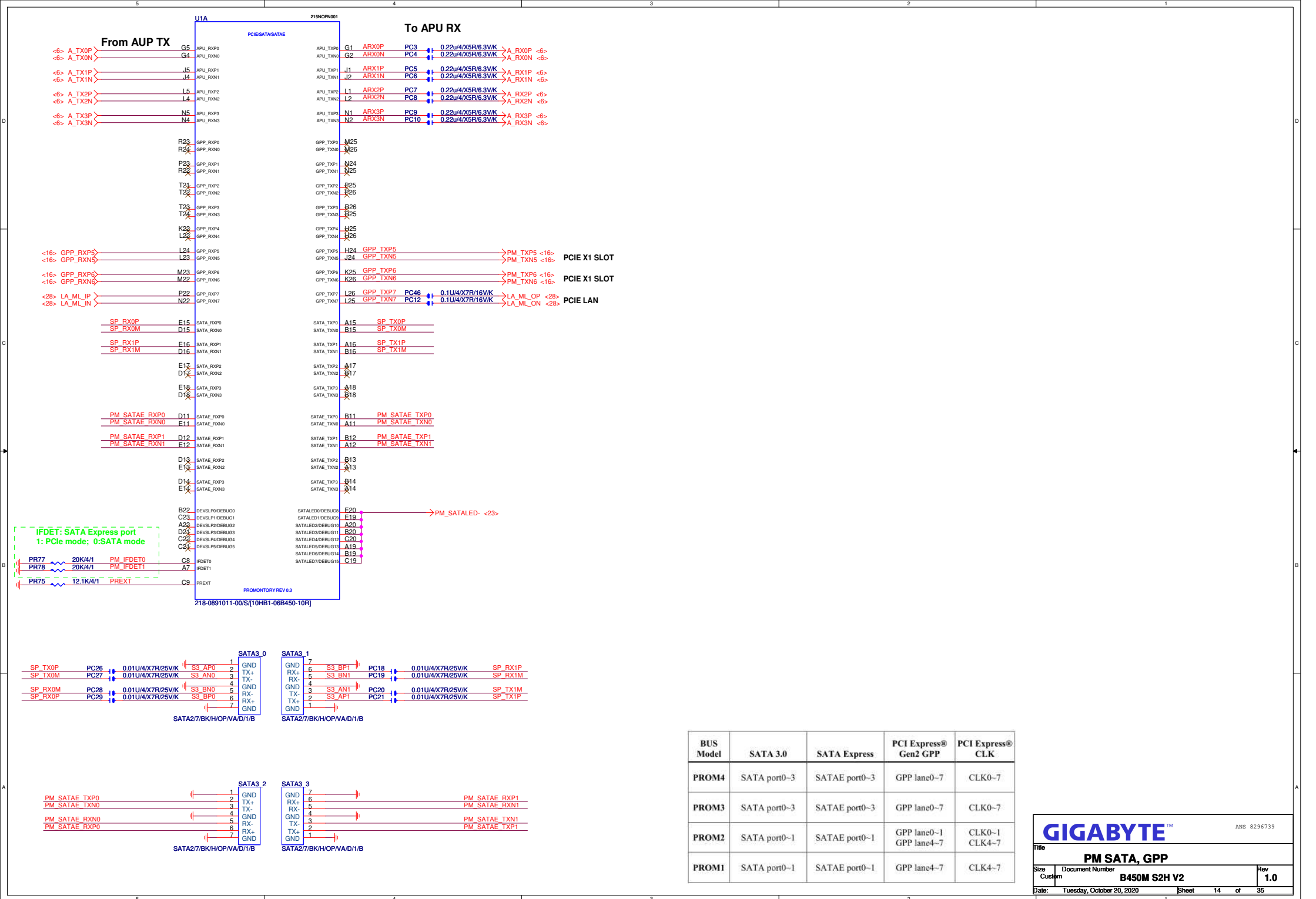




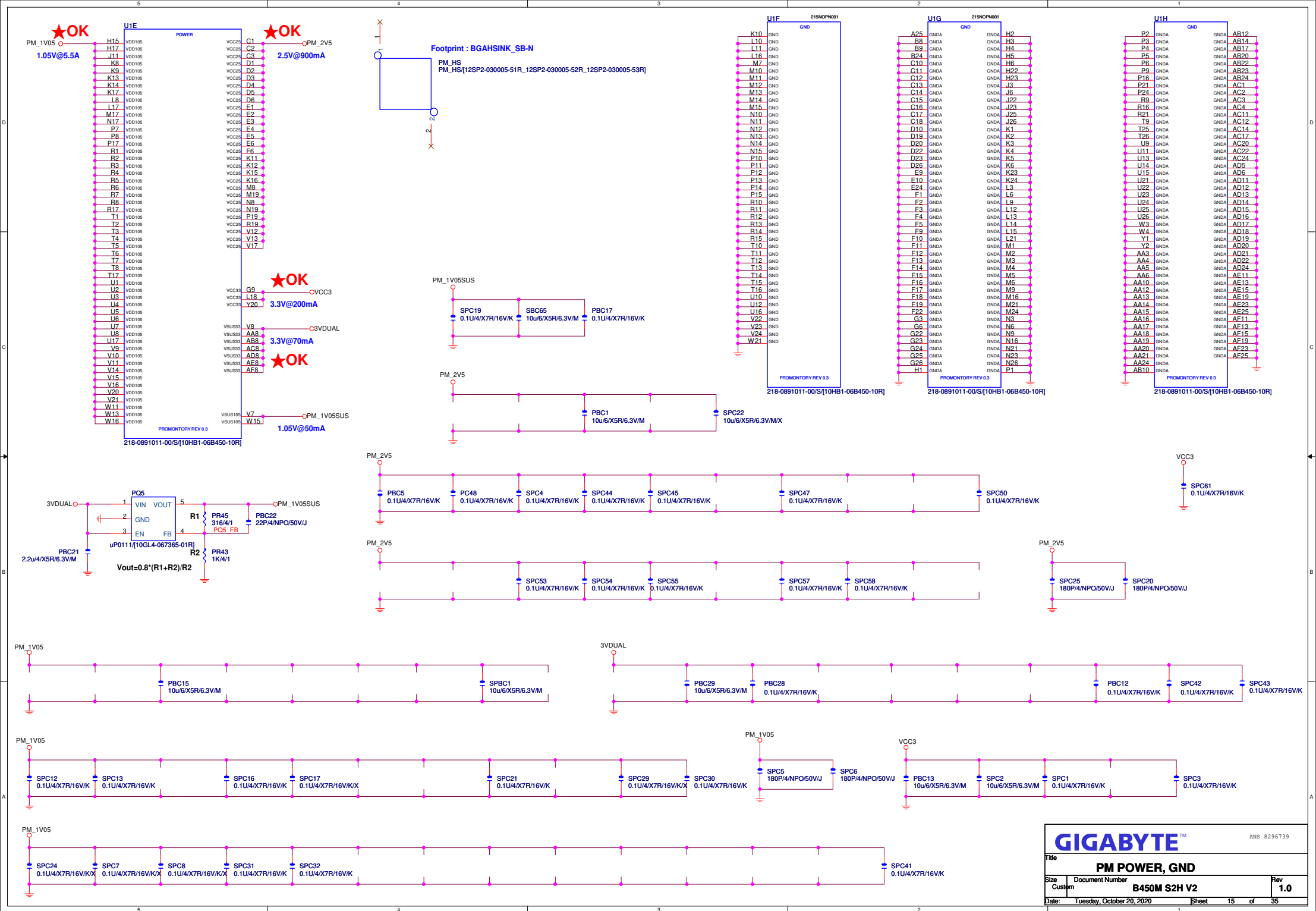




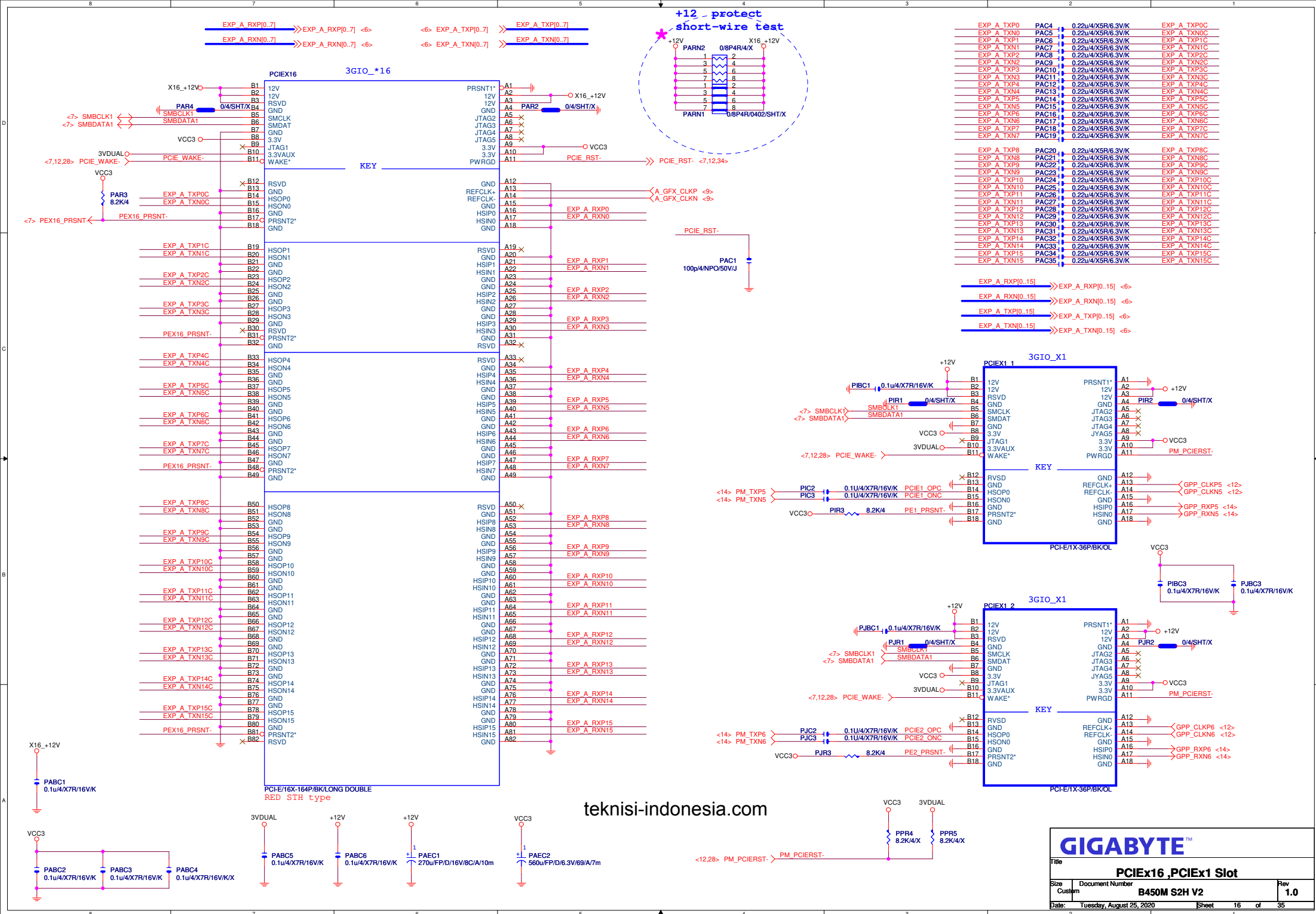




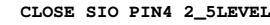






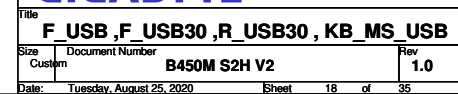
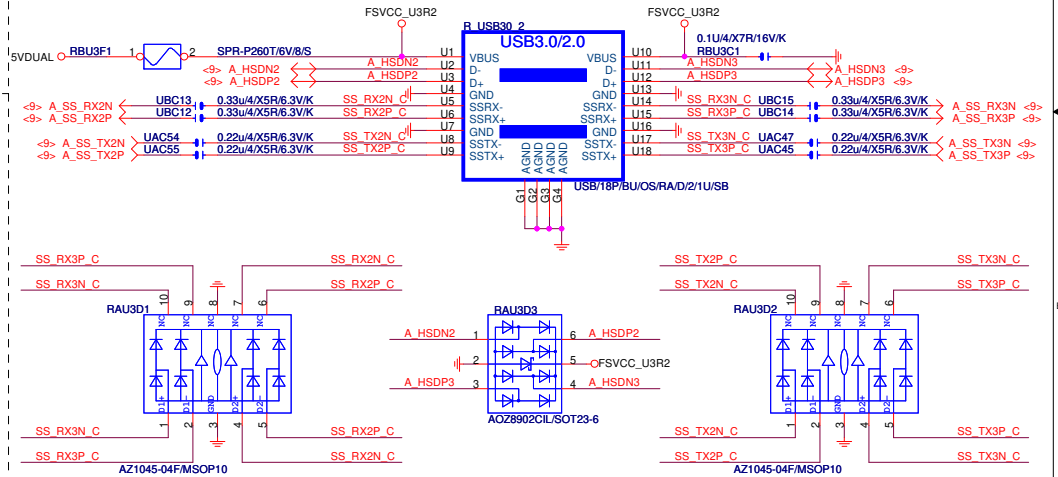
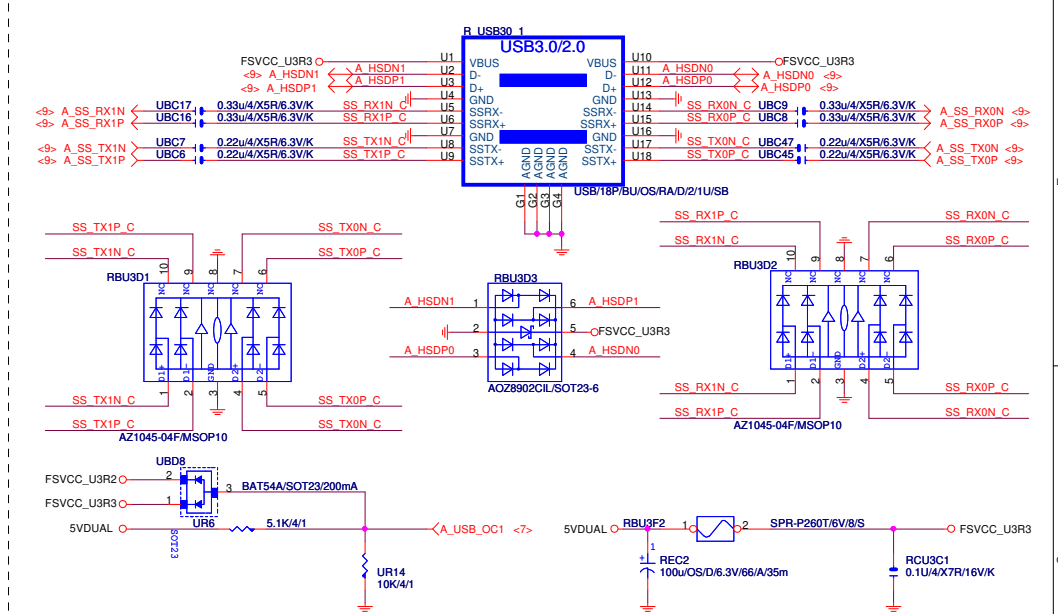
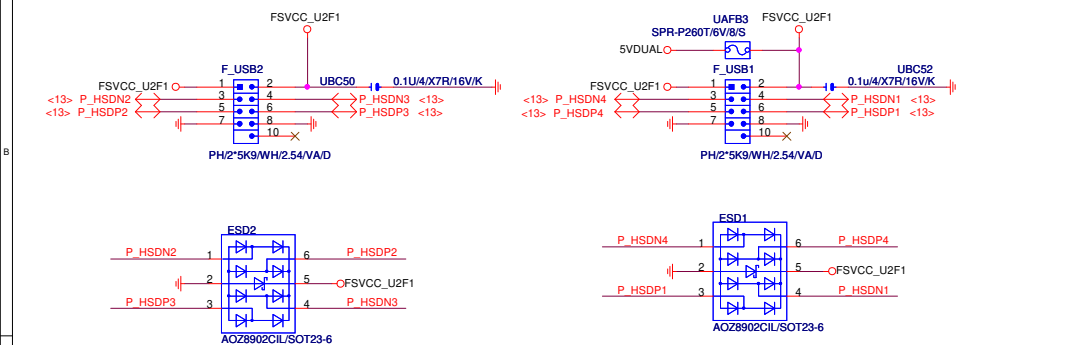








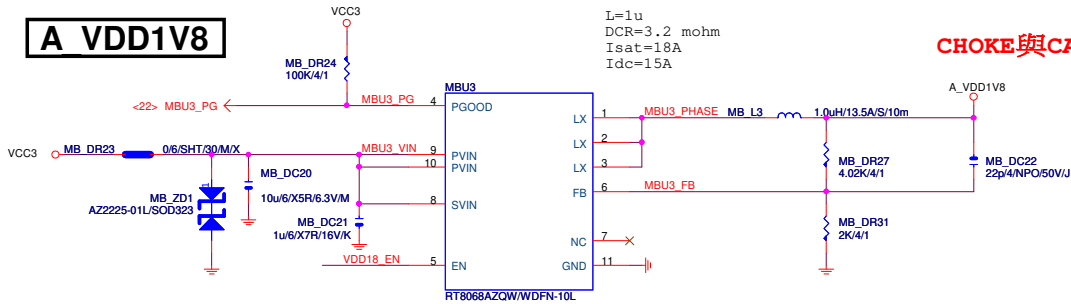
**FRONT SIDE USB2.0**





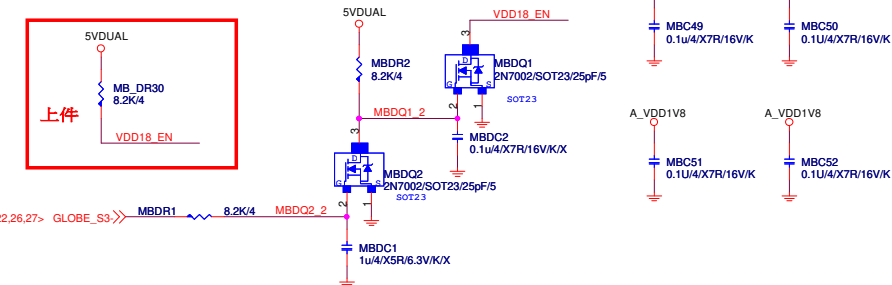
REV: 0.4

## A VDD1V8



### PWR\_SEQ

\* 刪 MA\_DR32



## VPP CAP

\* 大電容 ∞0

47u\*1PCS

GIGABYTE™

Title		
A_VDD1V8, A_VDDPS5		
Size	Document Number	Rev
Custom	B450M S2H V2	1.0
Date:	Tuesday, August 25, 2020	Sheet 19 of 35



Rev 3.0

# ALC887 三孔 AUDIO JACK

50歐姆: 4/5

Digital Area

Analog Area

50歐姆: 4/10

50歐姆: 4/10

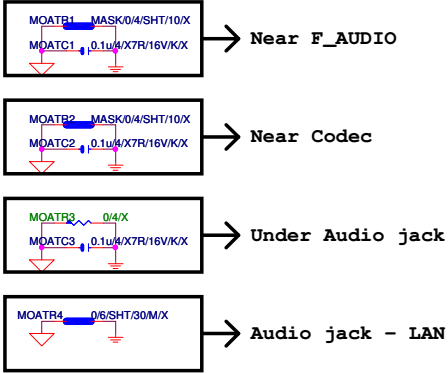
LAYOUT注意: 螺絲孔下GND方式

1. MH1空間夠, 下DGND  
空間不夠, 改為Isolate
2. MH2一律改為Isolate

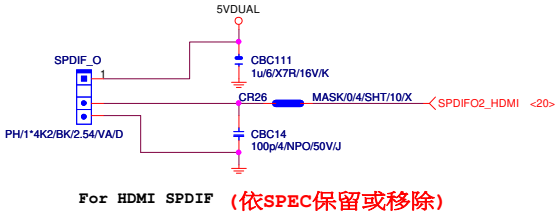
<input type="radio"/> MH1	<input type="radio"/> MH2
DGND	Isolate

www.teknisi-indonesia.com

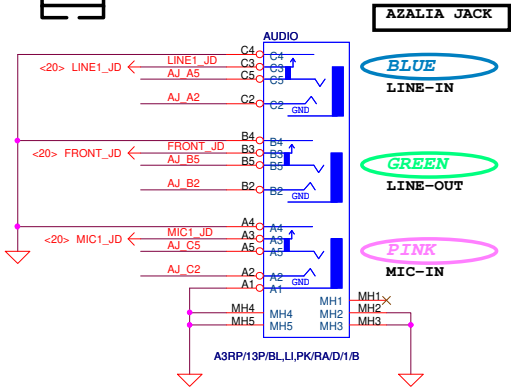
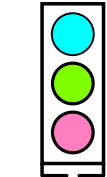




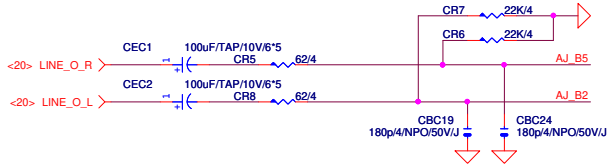
\*量産前, 0ohm改short pad



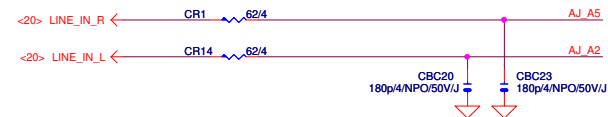
AZALIA JACK



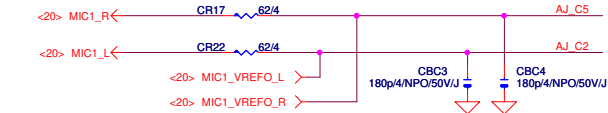
LINE-OUT



LINE-IN



MIC-IN

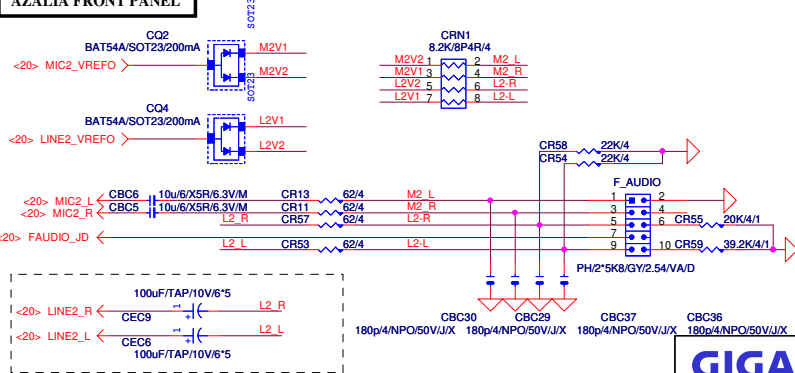


SURROUND

CEN/LFE

SURR BACK

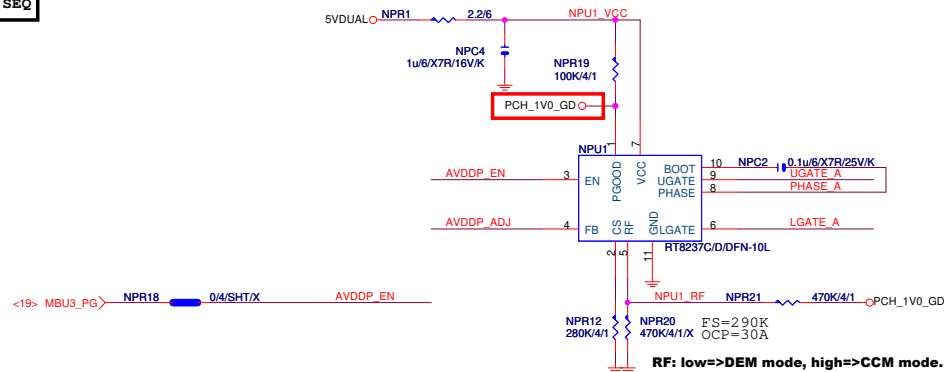
AZALIA FRONT PANEL



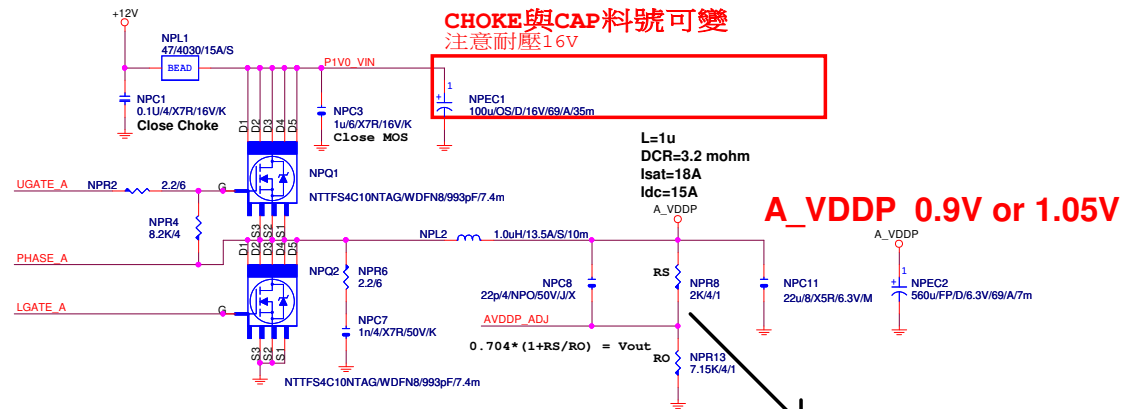
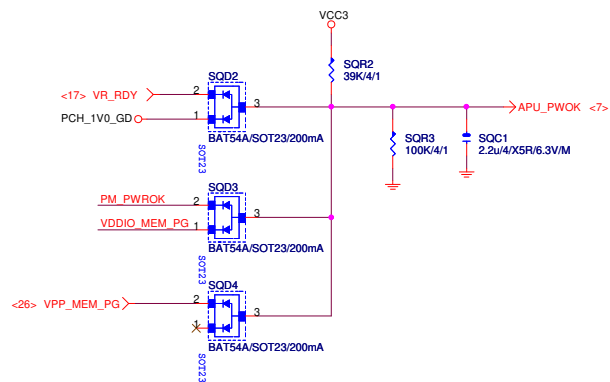
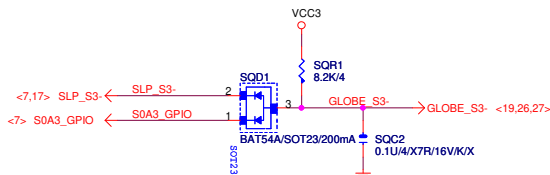
GIGABYTE™

AUDIO JACK



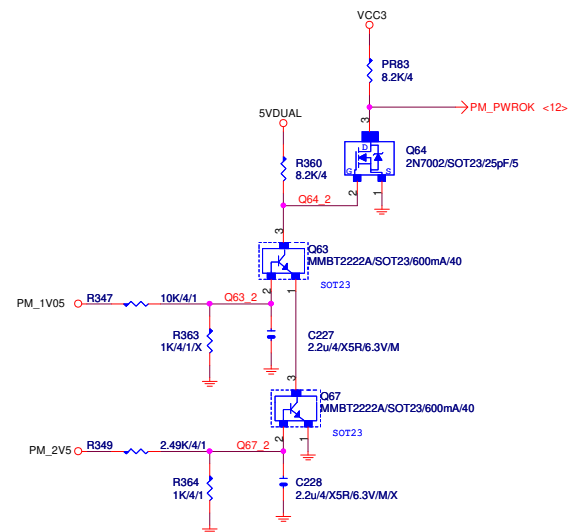
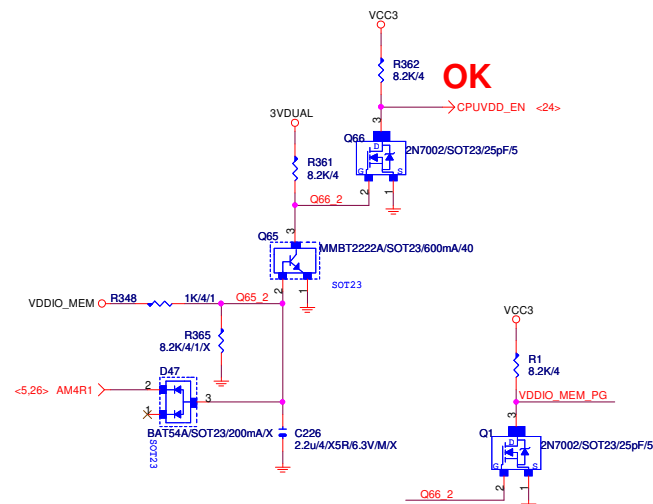


<19> MBUS3\_PG > NPR18 0/4/SHT/X AVDDP\_EN



CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

<5,7,19> CORETYPE1 < CORETYPE1 <5,7,19>



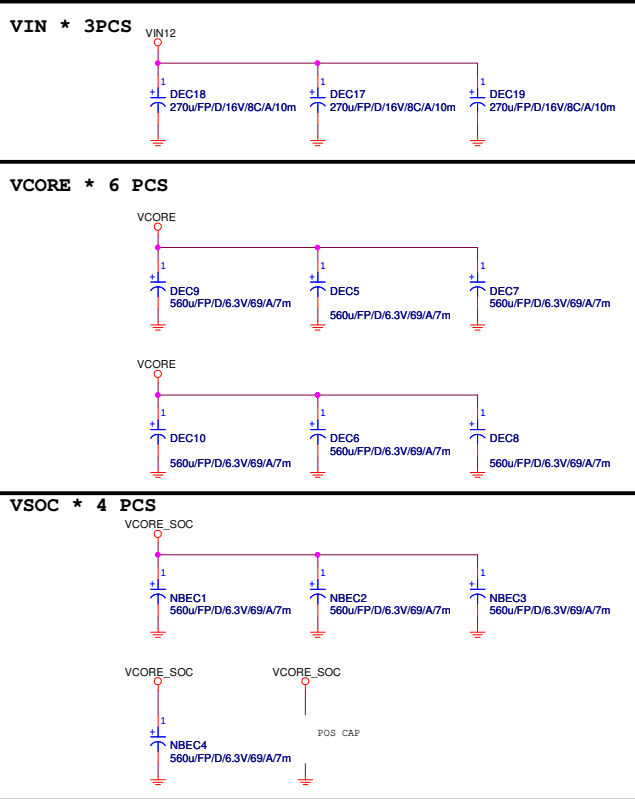
GIGABYTE™


POWER SEQ, A_VDDP		
Size	Document Number	Rev
Custom	B450M S2H V2	1.0
Date:	Tuesday, August 25, 2020	Sheet 22 of 35







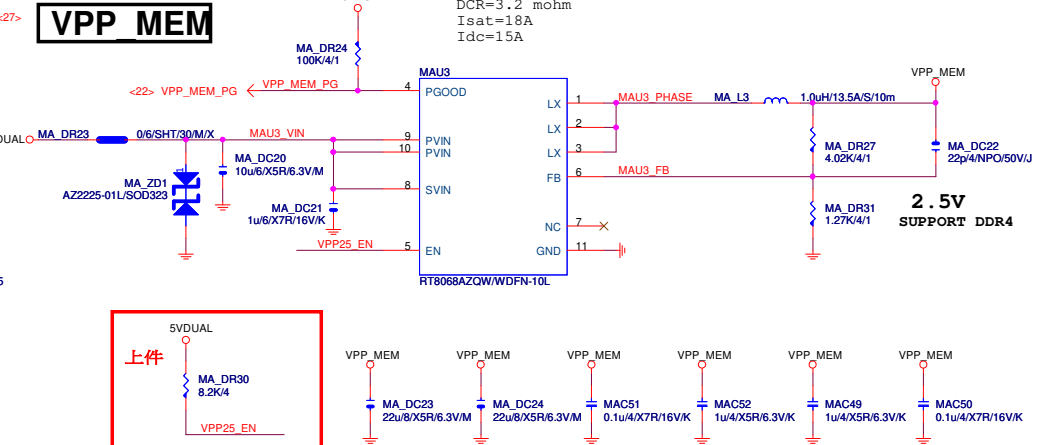
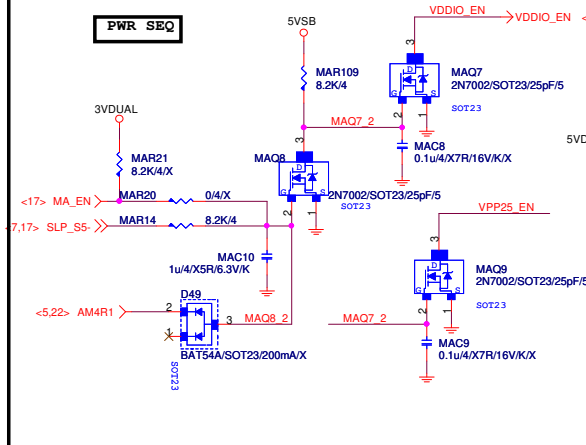
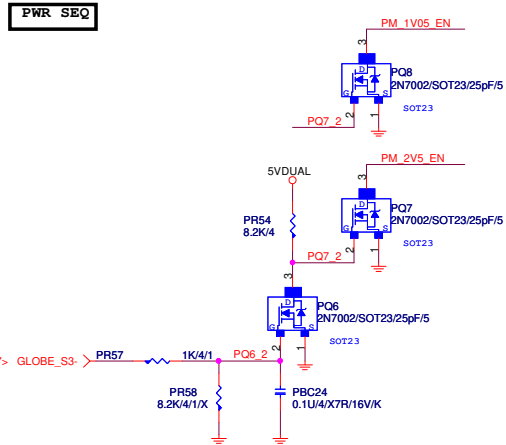
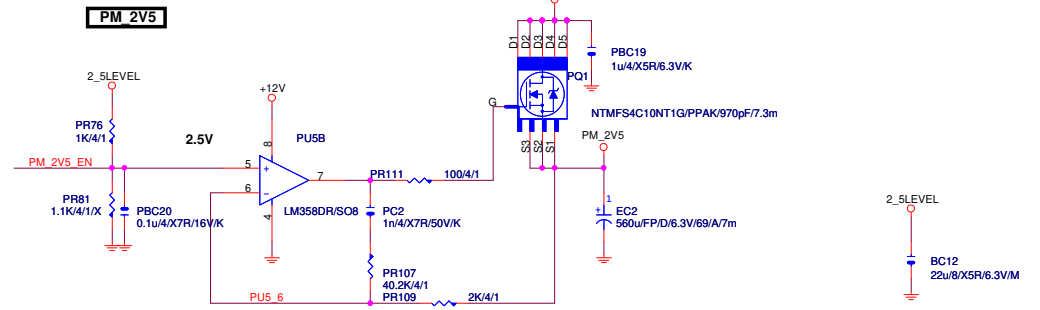
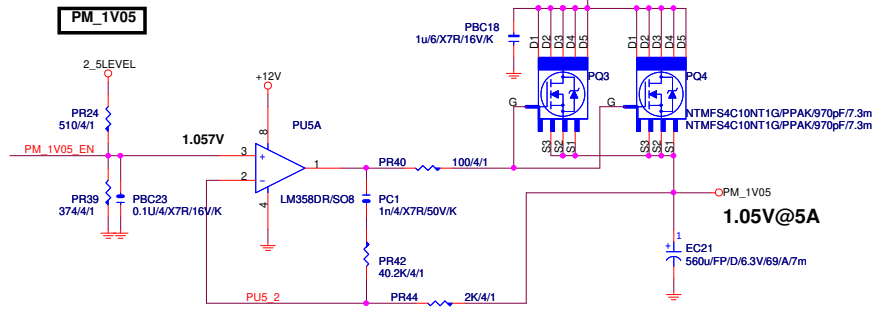
[illegible]

			
Title <b>VCORE (PWM ISL6277+6609A)</b>			
Size Custom	Document Number <b>B450M S2H V2</b>		Rev <b>1.0</b>
Date:	Friday, August 28, 2020	Sheet	24 of 35

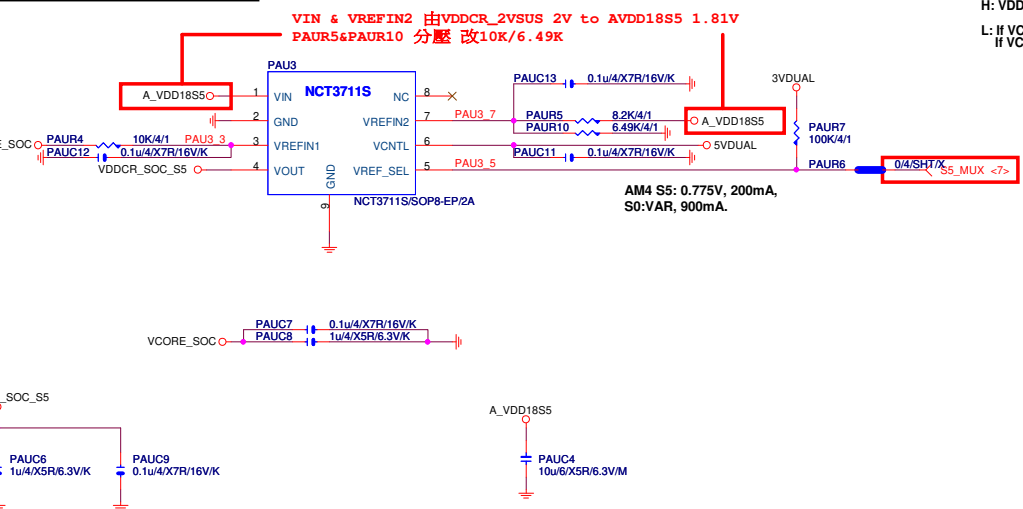




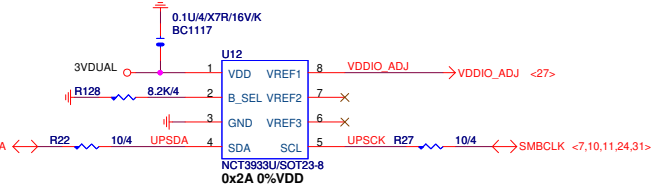




# VDDCR SOC S5



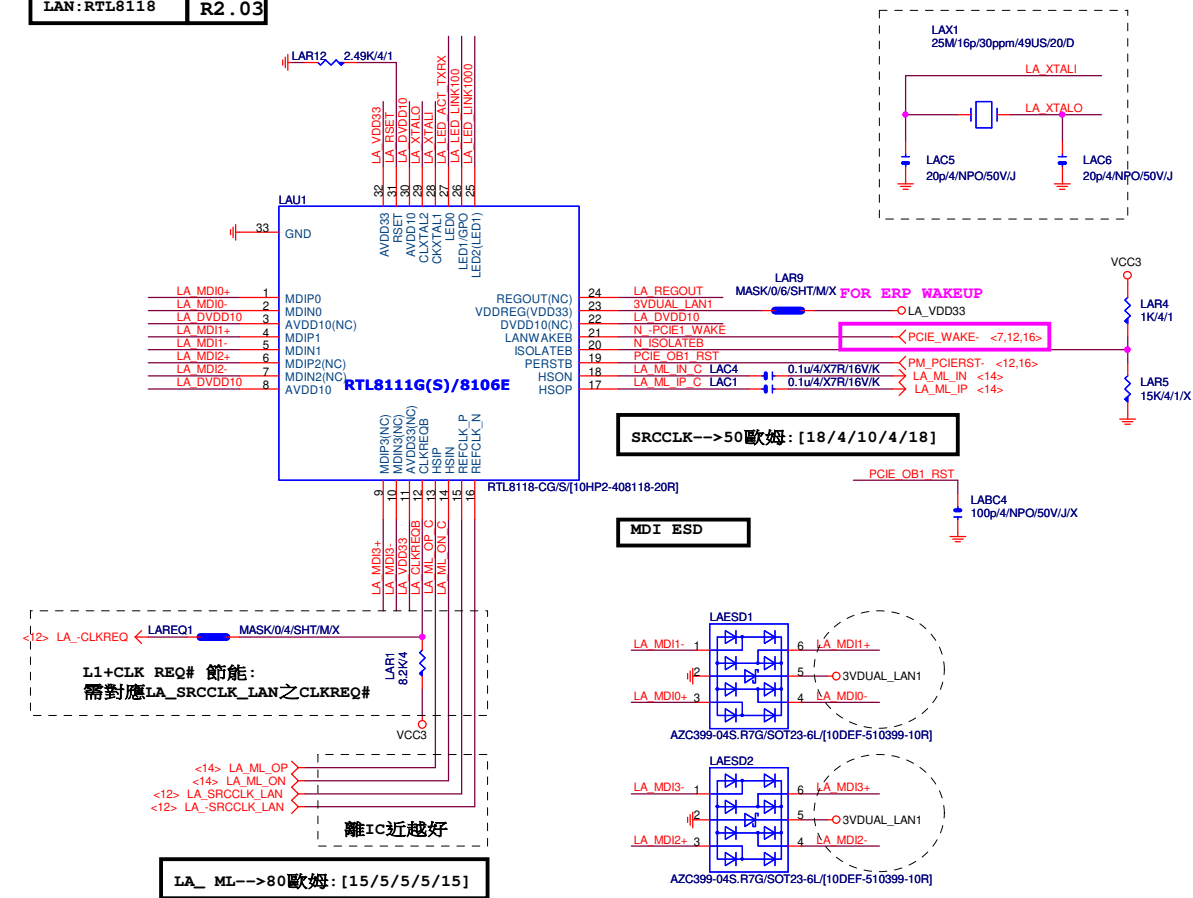
S5\_MUX: S0-->High, S5-->Low  
H: VDDCR\_SOC\_S5 will track VCORE\_SOC.  
L: If VCORE\_SOC < 0.775V (OR 0.85V), VDDCR\_SOC\_S5=0.775V.  
If VCORE\_SOC=0.775V (OR 0.85V), VDDCR\_SOC\_S5 will trace VCORE\_SOC.



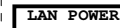
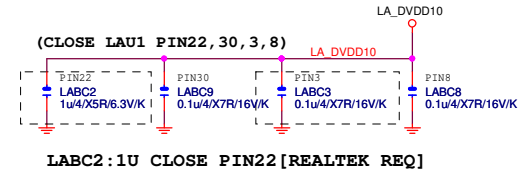
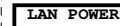




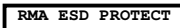
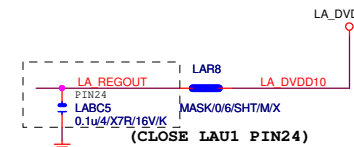
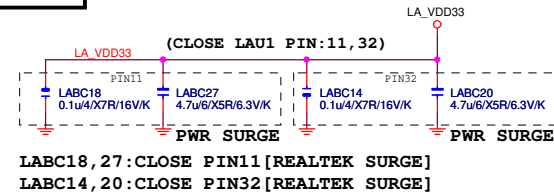
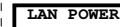
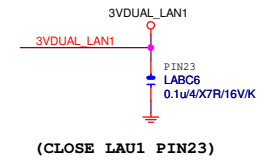




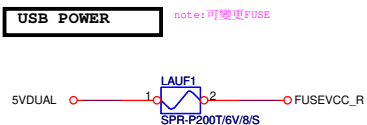
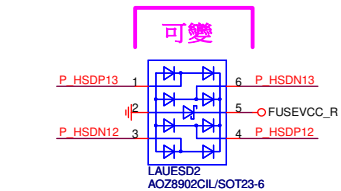
teknisi-indonesia.com



note: lan power連接及電流



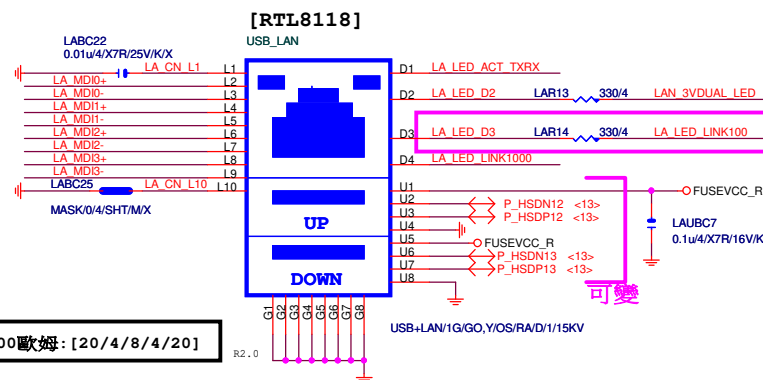
note:可變更USB NAME



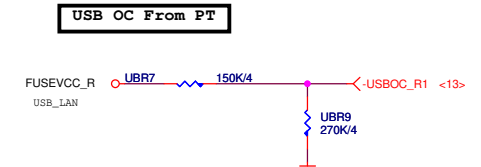
Close to connector  
USB\_LAN 2-Port 2.0A  
FUSE-0805



note:可變更USB NAME



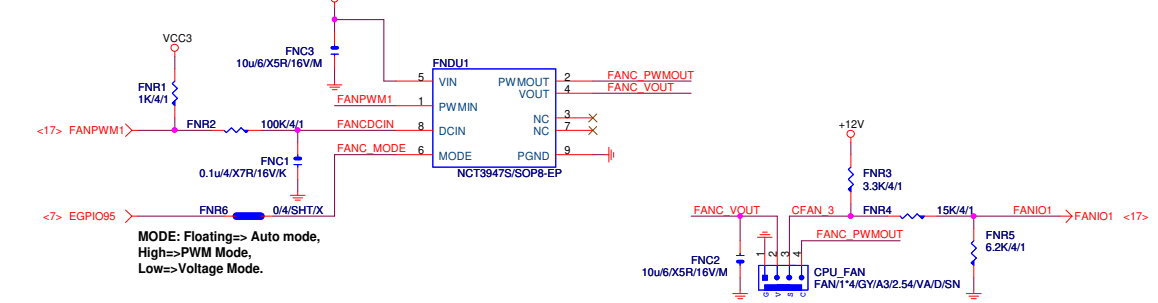
note: lan power連接及電流



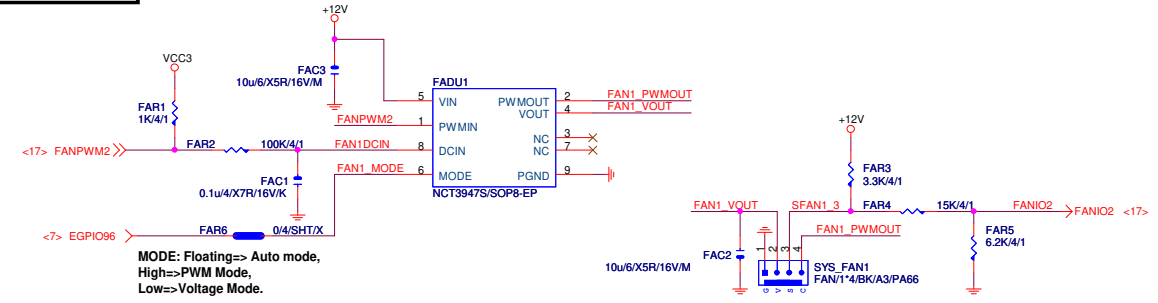
**GIGABYTE™**

Title			
RTL8118			
Size	Document Number	Rev	
Custom	B450M S2H V2	1.0	
Date:	Tuesday, August 25, 2020	Sheet	28 of 35

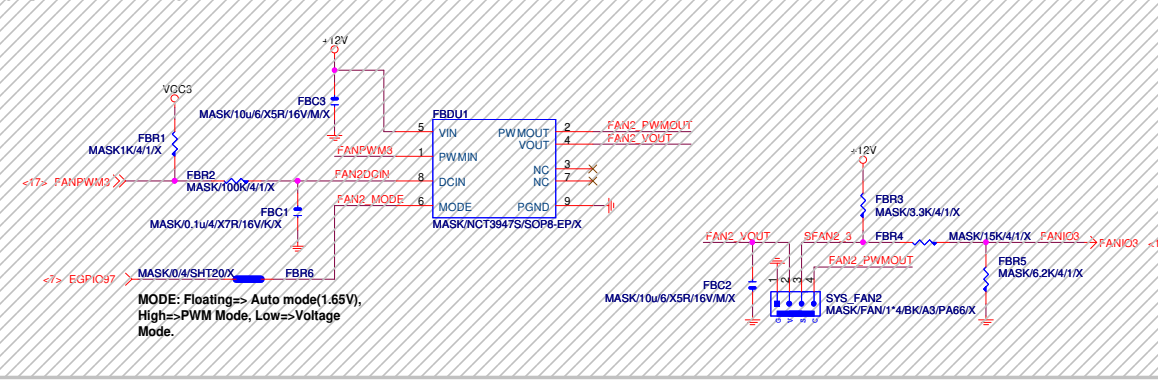




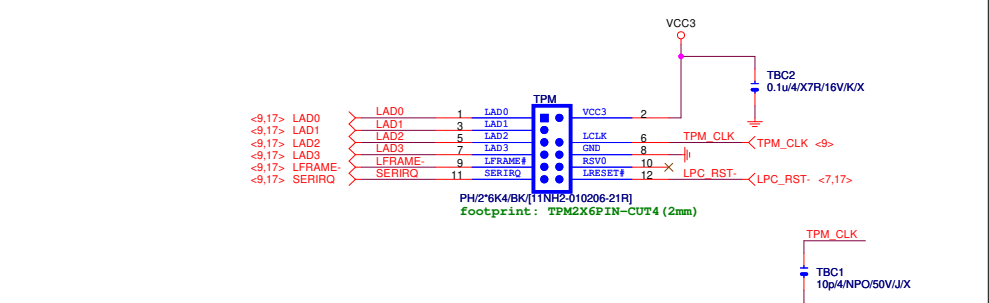
SYSTEM FAN1



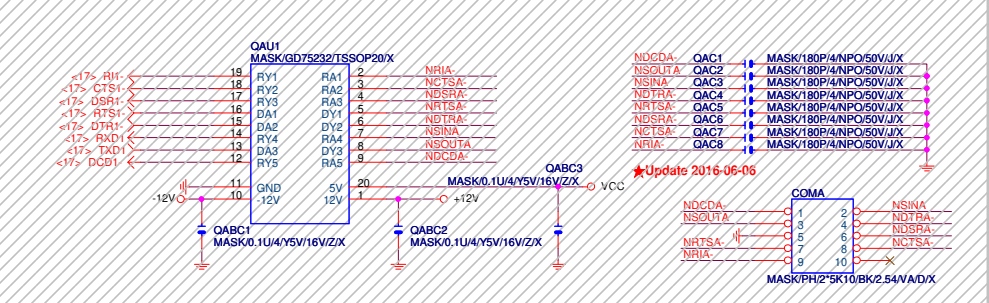
SYSTEM FAN2-MASK



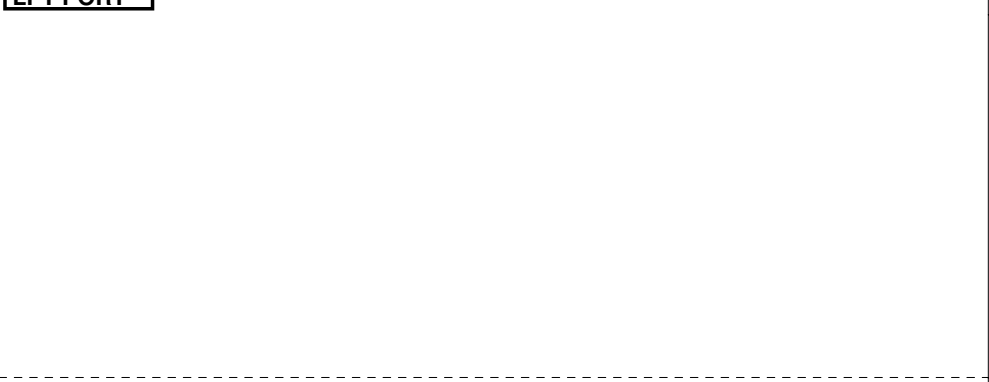
TPM



COM PORT-MASK

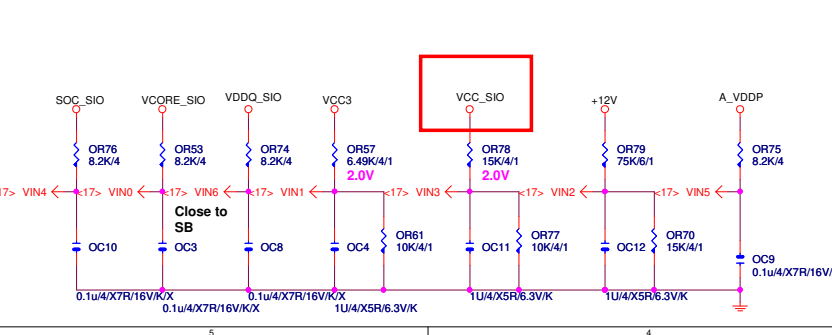


LPT PORT

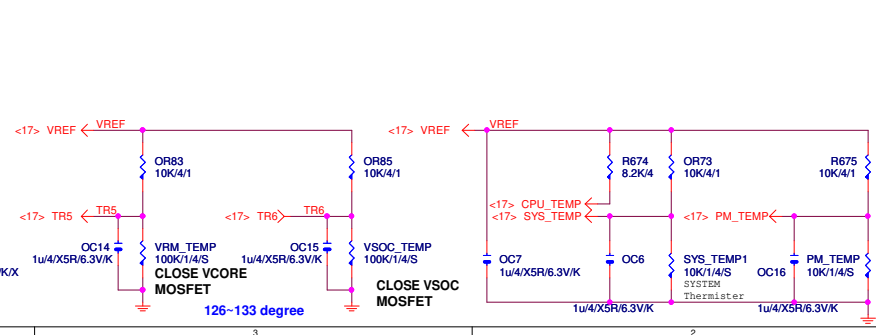


Hardware Monitor circuits - VOLTAGE

Rev:0.6



Hardware Monitor circuits - Temperature



**GIGABYTE**

Title: **FAN, LPT, COM, HWM**

Size: **B450M S2H V2**

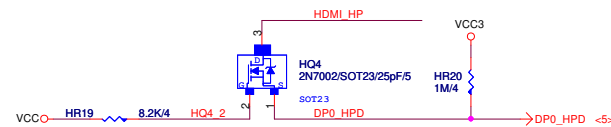
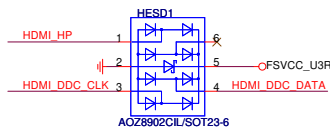
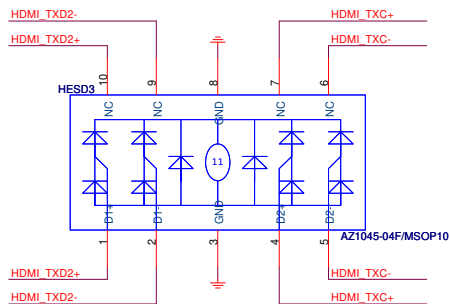
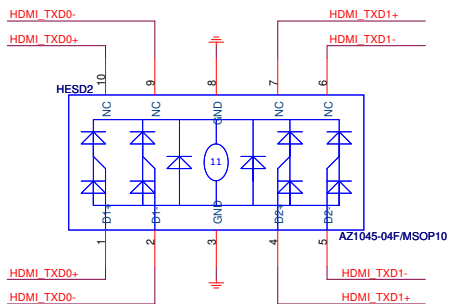
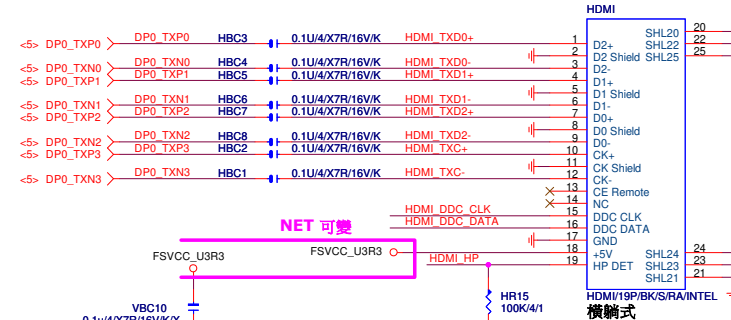
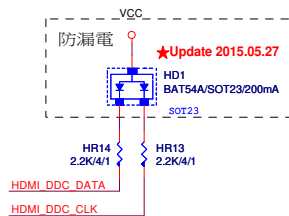
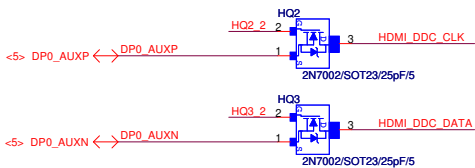
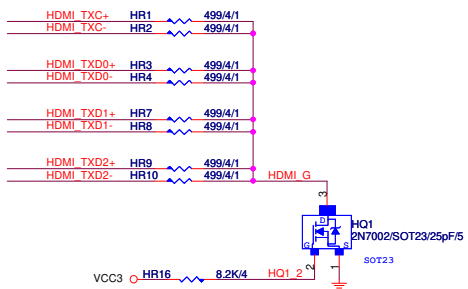
Document Number: **B450M S2H V2**

Rev: **1.0**

Date: **Tuesday, August 25, 2020**

Sheet: **29** of **35**

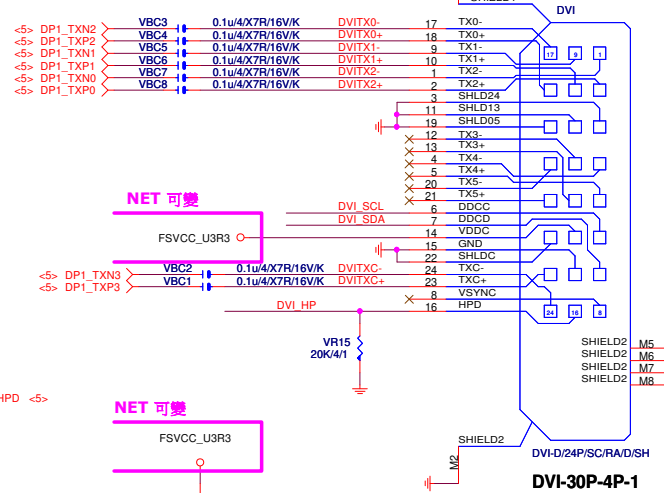
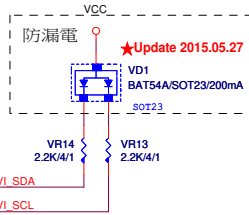
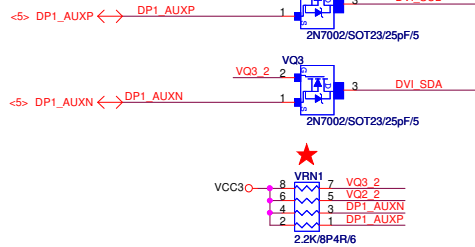
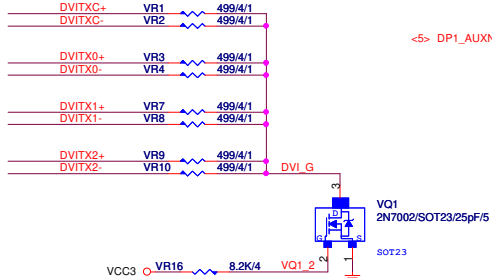




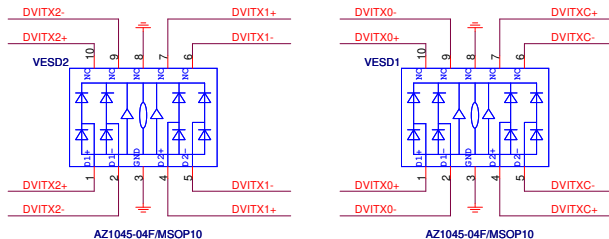
Rev: 0.73

DVI CONN

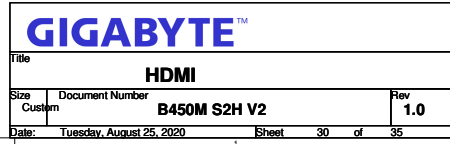
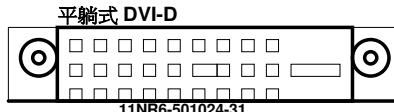
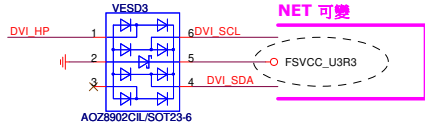
DVI: 20/4/6/4/20  
Impedance=85 +- 17.5%



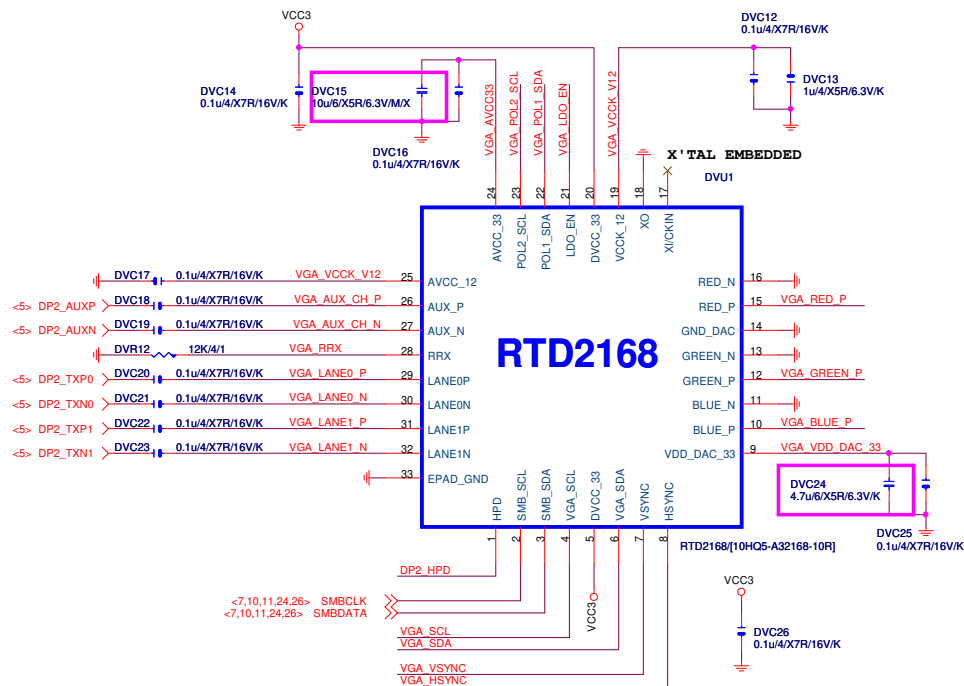
Close to connector



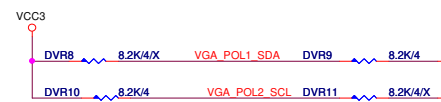
Close to connector







Power on latch



		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EP MODE
	1	<b>ROM ONLY MODE</b>	<b>EEPROM MODE</b>

## Embedded LDO

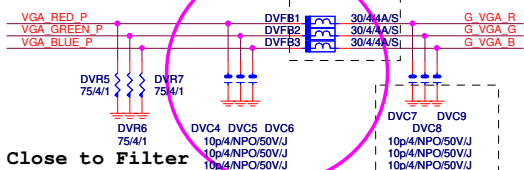
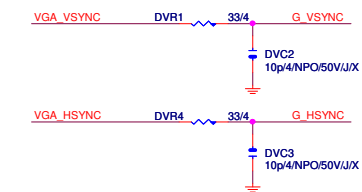


LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

DP HPD

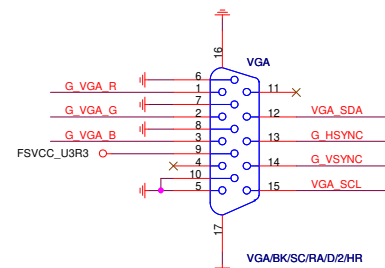
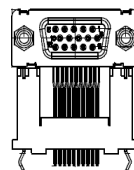
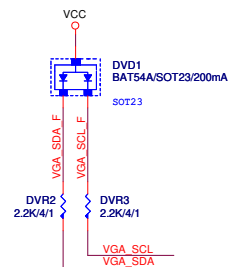


*Gigabyte Technology*

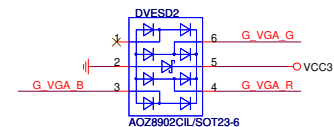
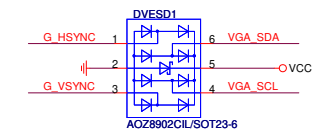


Close to Filter

FOR EMI



## VGA ESD



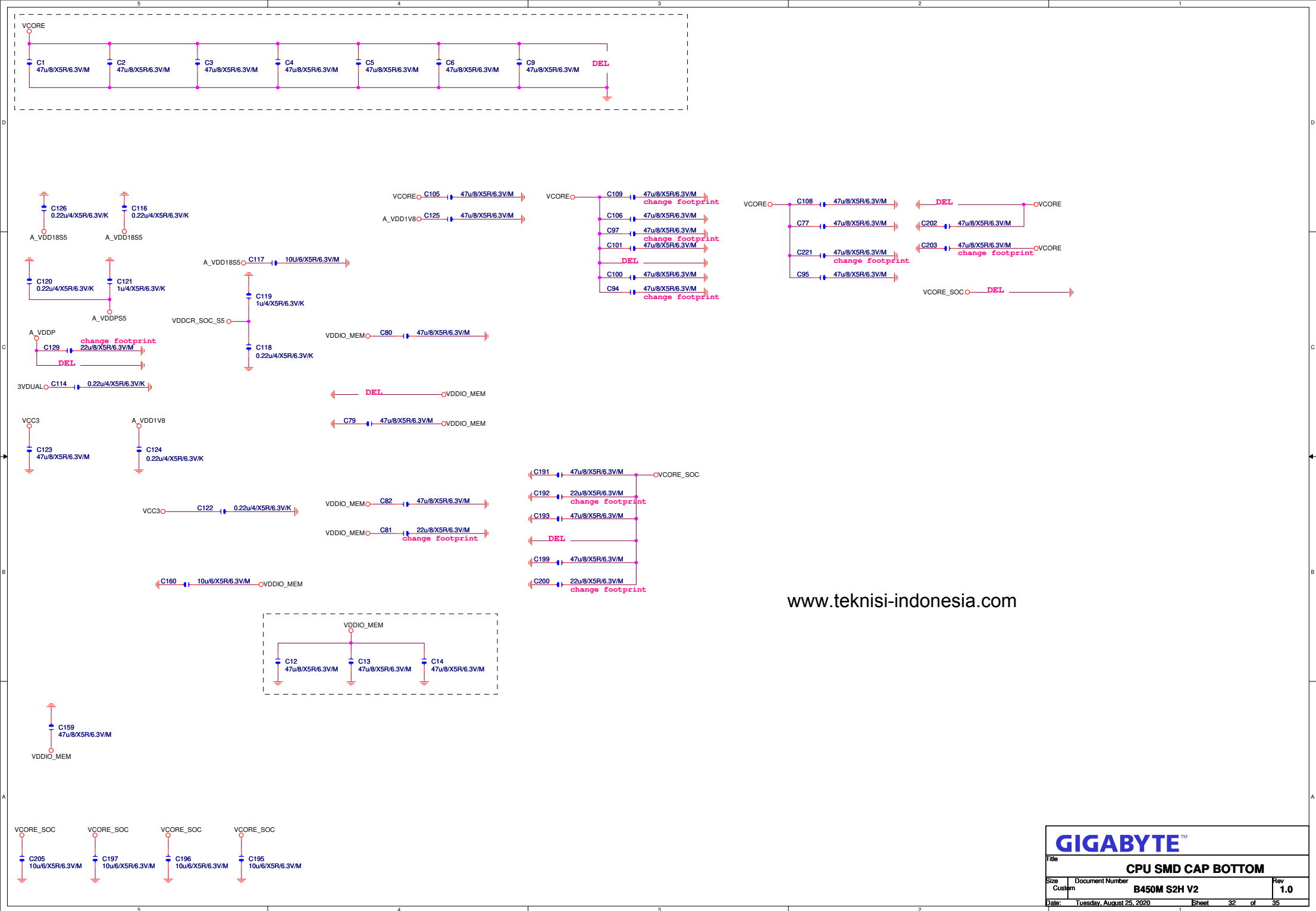
**GIGABYTE™**

## DP to VGA

**B450M S2H V2**

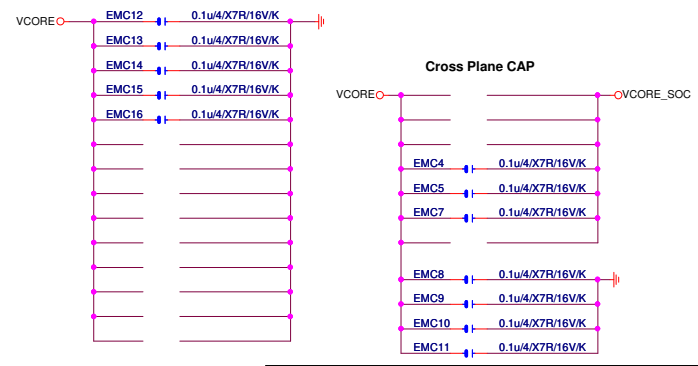
Rev	1.0
-----	-----





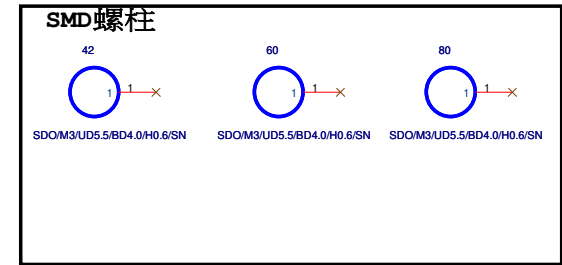
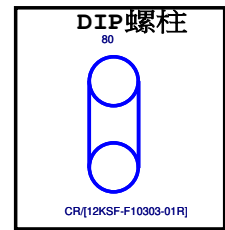
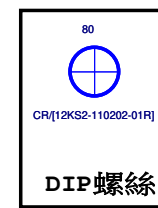
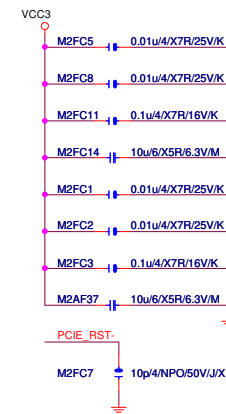
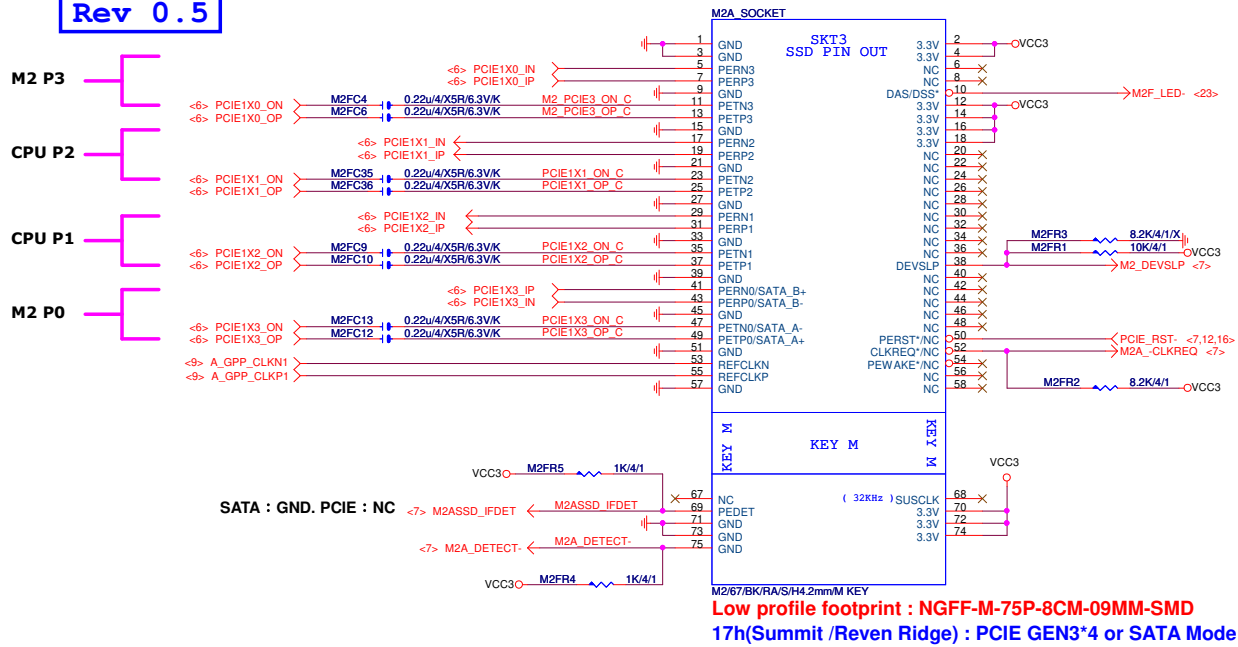


CPU TOP CAVITY

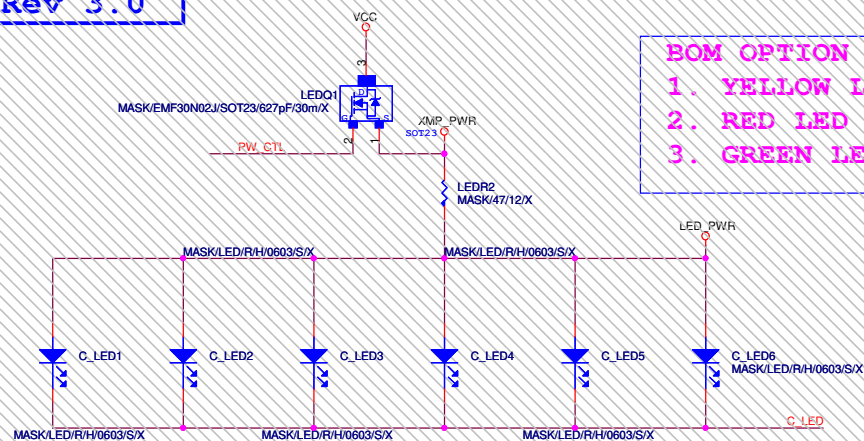




Rev 0.5







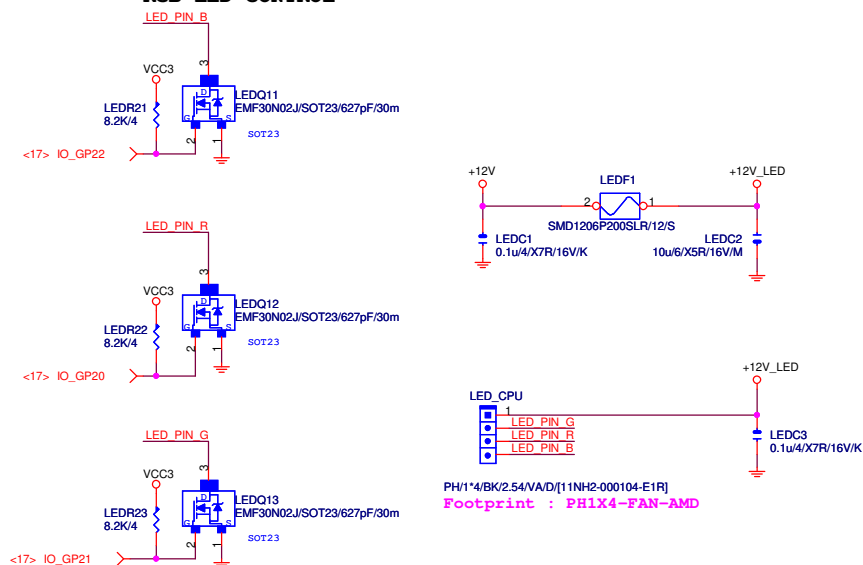
**BOM OPTION :**

1. YELLOW LED : LED/Y/6/M/S  
2. RED LED : LED/R/H/0603/S  
3. GREEN LED : LED/G/0603/S

## Ambient LED Control

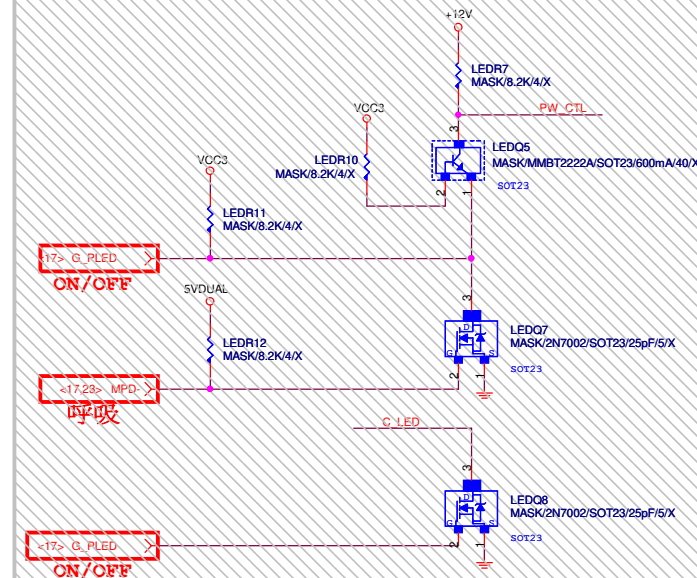
	IO_GP95	IO_GP91
Still Mode	H	L
OFF Mode	L	L
Pluse Mode	H	BREATH

## RGB LED CONTROL



## 三色 LED Control

	IO_GP20 (R)	IO_GP21 (G)	IO_GP22 (B)
Blue	L	L	H
Green	L	H	L
Light Blue	L	H	H
Red	H	L	L
Pink	H	L	H
Light Green	H	H	L
White	H	H	H
Cycle Mode	順序:Blue-Green-Light Blue- Red-Pink-Light Green-White 切換間隔時間為 1 秒		



teknisi-indonesia.com